

# InGaAs PSEUDOMORPHIC HEMTs FOR MILLIMETER WAVE POWER APPLICATIONS

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## ABSTRACT

We report the development of InGaAs pseudomorphic high electron mobility transistors with state-of-the-art power performance at millimeter-wave frequencies. Results include maximum power-added efficiencies of 44% at 35 GHz and 36% at 44 GHz, output power of 100 mW with 22% efficiency and 3 dB gain at 60 GHz, and output power of 9 mW at 94 GHz. Preliminary reliability data is presented, and prospects for further improvement in performance--the realization of multi-finger HEMTs capable of higher output power and reduction of gate length to 0.1  $\mu\text{m}$ --are discussed.

## INTRODUCTION

Over the past several years, HEMTs have exhibited unmatched transistor noise performance at frequencies ranging from 1 to 60 GHz [1]. More recently, it has become apparent that the devices are suitable for power applications as well. Power HEMTs based on the AlGaAs/GaAs heterojunction have been widely reported [2]-[6]. The InGaAs pseudomorphic HEMT, first demonstrated at millimeter-wave frequencies in 1986 [7], overcomes many of the limitations of the conventional AlGaAs/GaAs HEMT, allowing significantly improved power performance to be obtained.

## DEVICE DESCRIPTION

The conventional HEMT structure is described in [1]. The InGaAs pseudomorphic HEMT differs from the conventional HEMT in that a thin (typically 100-200 Å) layer of InGaAs is inserted between the donor AlGaAs layer and the buffer layer. Advantages of the InGaAs pseudomorphic structure include the enhanced electron transport properties of InGaAs, the large InGaAs/AlGaAs conduction band discontinuity which permits high two-dimensional electron gas (2DEG) sheet charge density, and improved confinement of carriers to the channel by the InGaAs quantum well. The HEMT enjoys the benefits of InGaAs, yet is still fabricated on a GaAs substrate and can be integrated into GaAs-based MMICs with little effort. However, since the InGaAs has a different lattice constant than GaAs, the layer must be kept sufficiently thin that the lattice strain is taken up coherently by the surrounding epi-layers, resulting in dislocation-free, "pseudomorphic" material. For  $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ , used in this work, the mismatch is only 1%, yet the strain might affect the long-term reliability of power transistors produced on this material. As discussed below, our preliminary reliability data suggests that HEMTs with strained layers can be reliable.

Carriers can be introduced into the InGaAs quantum well by doping on one or both sides of the InGaAs. The results reported here were obtained with both single heterojunction (doped above the InGaAs only) and double heterojunction (doped on both sides) devices. The single heterojunction pseudomorphic HEMT is similar to that described in [7]. The double heterojunction (DH) HEMT, shown in cross-section in Figure 1, contains several advanced features.

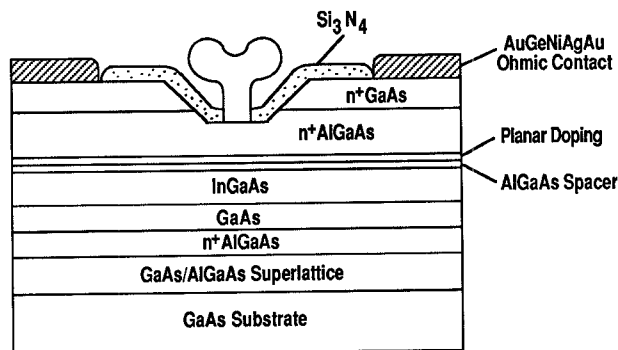


Figure 1. Cross-section of double heterojunction pseudomorphic HEMT.

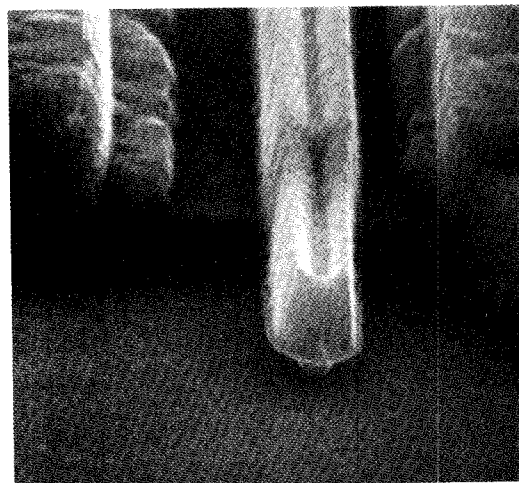
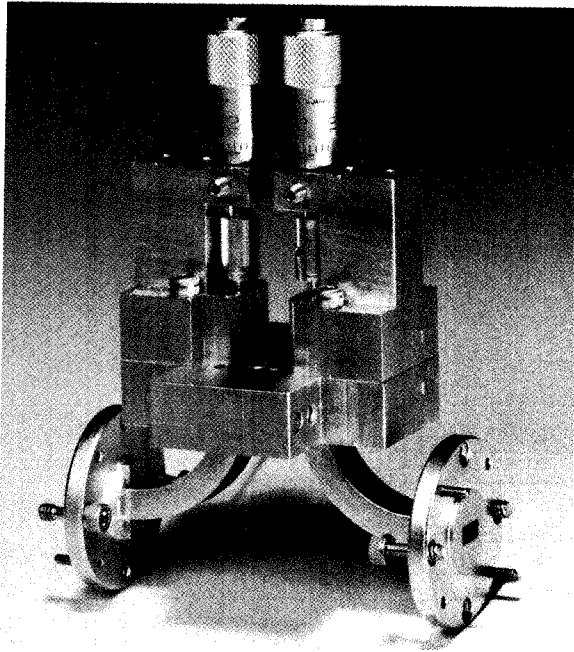


Figure 2. Channel region of 0.25  $\mu\text{m}$  HEMT.

Planar doping, in which a single atomic plane of Si atoms is deposited, has been used to obtain high sheet density while allowing a high gate length/gate-2DEG separation aspect ratio and low doping directly under the gate for high breakdown voltage. A superlattice buffer with doping in the uppermost AlGaAs layer was used, and the channel was coated with  $\text{Si}_3\text{N}_4$  dielectric. As shown in Figure 2, a 0.25  $\mu\text{m}$  long T-shaped gate, formed by electron-beam lithography using a tri-layer resist technique [8], is employed. The device geometry consists of a single gate stripe, fed at the center, with total gate widths of 50 and 150  $\mu\text{m}$ .



**Figure 3.** 44 GHz test fixture based on E-field probe waveguide/microstrip transition.

Frequency (GHz)	Output Power (mW)	Power Density (W/mm)	Power-Added Efficiency (%)	Power Gain (dB)
35	104	0.69	44*	5.0
	132	0.88*	30	5.0
44	100	0.67	36*	4.0
	126	0.84*	28	4.0
60	85	0.57	27*	3.3
	100	0.67*	22	3.0

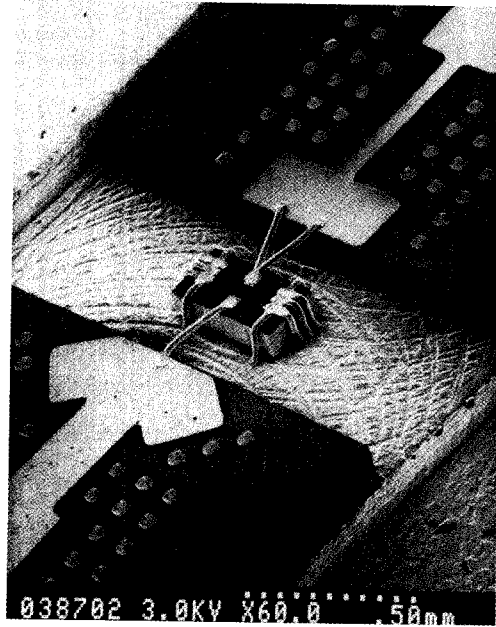
\*Biased and impedance-matched to maximize this parameter

**Table 1.** Measured performance of 0.25 x 150 $\mu$ m DH pseudomorphic HEMT.

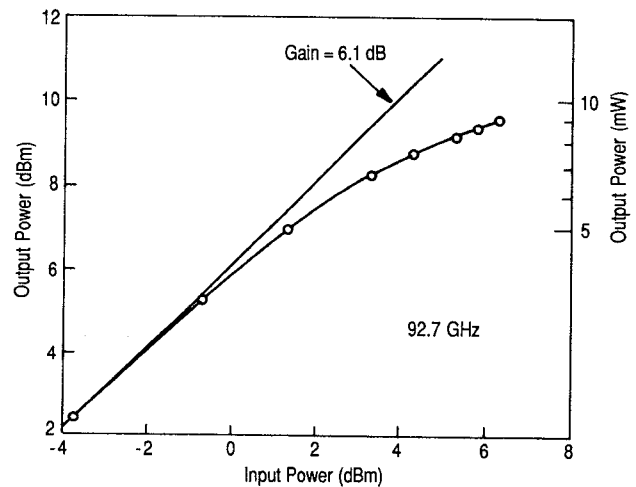
## DEVICE PERFORMANCE

The pseudomorphic HEMTs exhibit higher  $g_m$  than conventional HEMTs—500 mS/mm for the single heterojunction and 600 mS/mm for the double heterojunction devices. Full channel currents of 450 mA/mm and 600 mA/mm were measured for the single and double heterojunction HEMTs, respectively. A gate-drain breakdown voltage of approximately 9V is obtained for both device types.

Power measurements were performed at 35, 44, 60 and 94 GHz using E-field probe-type test fixtures such as the one shown in Figure 3. Such fixtures exhibit low insertion loss (0.5 dB at 44 GHz, for example) and a high degree of tunability. Single-stage amplifiers were constructed on fused silica using microstrip



**Figure 4.** 60 GHz test circuit for 0.25 x 150 $\mu$ m double heterojunction pseudomorphic HEMT.



**Figure 5.** Power saturation characteristic of 0.25 x 50 $\mu$ m pseudomorphic HEMT.

matching circuits designed with lower frequency S-parameter data, and tuned empirically for optimum performance. A 60 GHz test circuit is shown in Figure 4. All device test data reported here have been carefully corrected for test fixture loss.

Power test data at 35, 44 and 60 GHz for the 0.25 x 150 $\mu$ m DH pseudomorphic HEMT is given in Table 1. At each frequency, DC bias conditions and impedance matching were adjusted to separately maximize both output power and efficiency. As a result of their high current drive capability and high breakdown voltage, these HEMTs display very high power density—0.88 W/mm at 35 GHz, 0.84 W/mm at 44 GHz and 0.67 W/mm at 60 GHz. The output power at 60 GHz, 100 mW, is twice that reported earlier for conventional HEMTs of the same gate width [1].

When biased and tuned for maximum efficiency, the DH HEMTs exhibited state-of-the-art efficiencies of 44% at 35 GHz, 36% at 44 GHz, and 27% at 60 GHz. Although these efficiencies are comparable to those obtained for single heterojunction pseudomorphic HEMTs, the associated power densities and output power levels are significantly higher.

The 35 and 60 GHz power performance of 0.25 $\mu$ m single heterojunction pseudomorphic HEMTs fabricated in our laboratory was reported previously [1]. These devices have now been evaluated at 94 GHz. A maximum small-signal gain of 7.6 dB has been measured. The power saturation characteristic of this HEMT is plotted in Figure 5. Maximum output power is 9.1 mW with 3.3 dB gain and 12% power-added efficiency. With different DC bias and tuning, a maximum efficiency of 14% was obtained with 7.8 mW output power and 3.3 dB gain.

The current state-of-the-art of millimeter wave transistor efficiency is summarized in Figure 6. As seen in the figure, the pseudomorphic HEMT displays the highest efficiency reported across the entire 30-100 GHz frequency range.

While the small gate-width devices reported here have demonstrated record power levels at 60 and 94 GHz, requirements for much higher output powers can be met only by developing large gate-width, interdigitated power HEMTs. We have recently fabricated the 900 $\mu$ m gate-width HEMT shown in Figure 7. The device consists of two cells, uses air-bridge interconnects and via-hole source grounding, and is expected to generate an output power of 0.5 Watt with high efficiency at frequencies as high as 44 GHz.

Unit gate finger width is crucial in determining ultimately how much power a FET or HEMT can deliver. Using the T-shape gate structure allows longer fingers, or alternatively, provides higher gain and efficiency for the same finger width, than conventional gate structures. The gain degradation due to gate line attenuation was calculated for both types of gate structures using a transmission line model [12], and is compared in Figure 8.

## RELIABILITY

Preliminary reliability testing of the DH pseudomorphic HEMT has been conducted. Devices stored at 250°C exhibit a 10% degradation in transconductance after 300 hours. A DC life test in which the device was biased for power operation was performed at a channel temperature of 250°C, with failure occurring at 100 hours. The results are encouraging, since they are comparable to those obtained for low noise AlGaAs/GaAs HEMTs. If an activation energy of 1.5 eV is assumed (as determined for conventional HEMTs [1]), then MTTF of 10<sup>6</sup> hours is expected at a channel temperature of 135°C, and with careful thermal design, pseudomorphic HEMTs should be sufficiently reliable for many power applications. More reliability work, including RF life testing at several temperatures and failure analysis, is needed.

## 0.1 $\mu$ m DEVICES

Reduction of gate length below 0.25 $\mu$ m is expected to further improve device gain, and hence efficiency due to increased transconductance as well as lower input capacitance. The 0.1 $\mu$ m gate length single heterojunction pseudomorphic HEMT shown in Figure 9 has yielded extrinsic transconductance of 930 mS/mm, and small-signal gain of 6.7 dB at 94 GHz [10] despite extremely high gate resistance (1700 $\Omega$ /mm). Equivalent circuit modeling indicates that a 3 dB improvement in gain would result from the use of a 0.1 $\mu$ m T-gate structure, and such devices, when developed, promise excellent gain and efficiency at frequencies as high as 94 GHz.

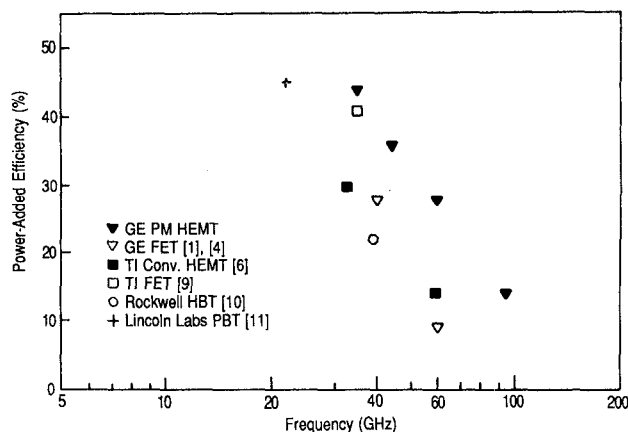


Figure 6. Best reported millimeter-wave transistor efficiencies.

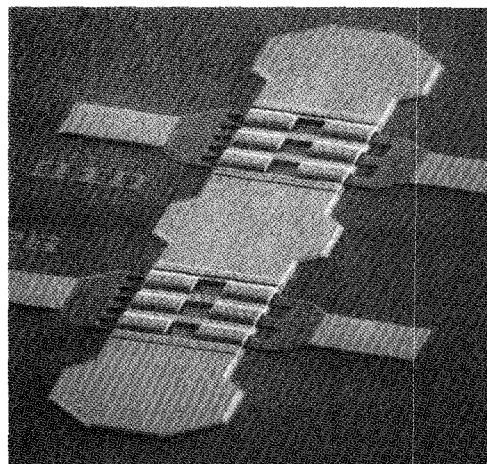


Figure 7. 0.25 x 900 $\mu$ m power HEMT.

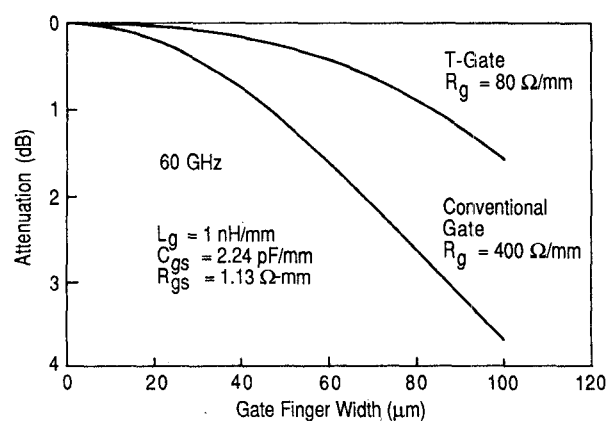


Figure 8. Comparison of gate line attenuation for 0.25 $\mu$ m T-gate and conventional gate structures.

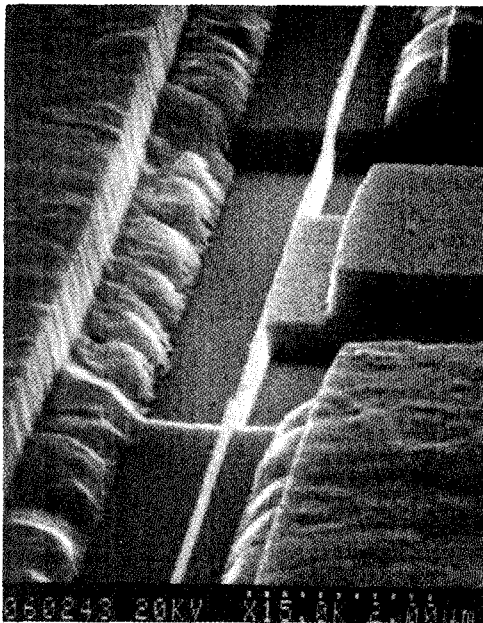


Figure 9. 0.1 $\mu$ m gate-length pseudomorphic HEMT.

## SUMMARY

InGaAs pseudomorphic HEMTs have demonstrated unprecedented transistor power performance at millimeter-wave frequencies, simultaneously providing high power density and high efficiency. Moreover, initial reliability work suggests that HEMTs with strained layers can be reliable.

Future device development will focus in several areas: the realization of large gate-width multi-finger HEMTs capable of much higher output power, optimization of the layer structure and reduction of gate length for improved performance, and reliability testing to guide the design of reliable power HEMTs.

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